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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,154	07/11/2000	Martin J. Edwards	PHB 34,365	1602

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EXAMINER
SHAPIRO, LEONID

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/614,154	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 July 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. This application has been filed with informal drawings are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

3. The drawings are objected to because, in Fig. 4. there are no connections between converter circuit blocks 9, 8, 7, 6 to bus lines 45. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 5 objected to because of the following informalities: On line 2 – "analogue'. Should be change to 'analog'. Appropriate correction is required.

Specification

5. The disclosure is objected to because of the following informalities: On page 11, Line 26 should be multiplexing circuit 31, instead 30.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-5 rejected under 35 U.S.C. 102(e) as being anticipated by Matsueda et al. (US Patent 6,384,806 B1).

As to claim 1, Matsueda et al. teaches an active matrix array device with an array of individually addressable matrix elements, first and second sets of crossing address conductors connected to the matrix elements and the sets of address conductors being carried on a substrate (See Fig. 15-17, items 10, 100, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58) and an addressing circuit connected to the sets of row and column conductors for addressing the matrix elements which addressing circuit comprises a multiplexing circuit (inside of 10A and 10B, Fig. 17) integrated on the substrate and connected to the first set of conductors and having a plurality, n, of signal bus lines , the address conductors of the first set being arranged in a series of groups with each group comprising n successive address conductors

and the multiplexing circuit (inside of 10A and 10B, Fig. 17) being arranged to couple sequentially each group of address conductors to the signal bus lines with each address conductor in a group being coupled to a respective one of the bus lines, the addressing circuit further including a respective signal processing circuit connected to each bus line, characterized in that the signal processing circuits associated with the bus lines are integrated as respective circuit blocks on the device substrate with the individual signal processing circuit blocks associated with adjacent column conductors being located close together on the device substrate (See Fig. 15-17, items 10, 100, 101, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58)

As to claim 2, Matsueda et al. teaches an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-45). Notice that D/A converters on both sides of LCD panel.

As to claim 3, Matsueda et al. teaches an active matrix array device with the multiplexing circuit (inside of m/2-bit shift registers) extends alongside one (two) edges of the array of matrix elements and the signal processing circuit blocks are arranged in at least one (two) row(s) extending alongside the multiplexing circuit (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-48). Notice that multiplexing circuits are in the shift registers on both sides of LCD panel.

As to claim 4, Matsueda et al. teaches an active matrix array device with matrix elements are electro-optic circuits (See Fig. 15-17, in description See Col.19, Lines 14-18).

As to claim 5, Matsueda et al. teaches an active matrix array device with the signal processing circuits comprise digital to analog converter circuits (See Fig. 17, items 101B, 101A, in description See Col.19, Lines 58-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda et al. as aforementioned in claim 4 in view of Okumura (US Patent 5,751,279).

Matsueda et al. does not teach an active matrix array device with the signal processing circuits comprise sample and hold circuits.

Okumura shows the sample and hold circuits in the active matrix type liquid crystal display (See Fig. 3, item303, in description See Col. 6, lines 21-34). It would have been obvious to one of ordinary skill in the art in the time of invention to incorporate the sample and hold circuit as shown by Okumura in the Matsueda et al. apparatus in order to minimize the space for the signal processing circuits.

7. Claims 7-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda et al. as aforementioned in claims 1-3 in view of Zhang et al. (US Patent No. 6,255,705 B1).

As to claim 7, Matsueda et al. does not teach an active array device with matrix elements comprise sensing elements each responsive to an input to produce an output signal along its associated address conductor of the first set.

Zhang et al. shows an active matrix-type area image sensor circuit (See Fig. 3(a), items 353-354, in description See Col.15, Lines 61-65). It would have been obvious to one of ordinary skill in the art in the time of invention to incorporate an active matrix-type area image sensor circuit as shown by Zhang et al. in Matsueda et al. apparatus in order to improve the image quality an active matrix-type area image sensor.

As to claim 8, Matsueda et al. and Zhang et al. do not teach an active matrix array device with the sense amplifier as part of the signal processing circuits. I t is well known in the art that sense amplifier would be used for an active matrix-type area image sensor, for example CCD cameras. It would have been obvious to one of ordinary skill in the art in the time of invention to incorporate an amplifier in Zhang et al. and Matsueda et al. apparatus in order to improve the image quality an active matrix-type area image sensor.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Sasaki (US Patent No. 6,049,321) reference discloses the sample and hold circuit for liquid crystal display.

The Nakamura et al. (US Patent No. 6,411,273 B1) reference discloses drive circuit for active matrix liquid crystal display.

The Maekawa (US Patent No. 6,256,124 B1) reference discloses DAC circuit for liquid crystal display.

The Matsueda et al. (US Patent No. 6,380,917 B2) reference discloses driving circuit for liquid crystal display.

The Gorny et al. (US Patent No. 6,326,958 B1) reference discloses power partitioned miniature display system.

The Lewis (US Patent No. 5,589,847) reference discloses switched capacitor analog circuits using polysilicon thin film technology.

The Ozawa (US Patent No. 6,380,920 B1) reference discloses electro-optical device drive circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

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October 18, 2002

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
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